PERMANENT
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KENNY UMENTHUM

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CURRENT
504 E Clark #14
CHAMPAIGN, IL 61820

EDUCATION

UNIVERSITY OF ILLINOIS AT URBANA CHAMPAIGN
BACHELOR OF SCIENCE (MAY 2016, 3.37)
–IN ELECTRICAL ENGINEERING
–IN MATHEMATICS & COMPUTER SCIENCE
MASTER OF SCIENCE IN ELECTRICAL AND COMPUTER ENGINEERING (MAY 2018)

INTERESTS

EDA, VLSI, HLS, FPGA, architecture, compilers and programming languages

EXPERIENCE

UNIVERSITY OF ILLINOIS, URBANA, IL (FALL 2016 - CURRENT)

- Teaching assistant for ECE411, Computer Organization & Design

NATIONAL TSING HUA UNIVERSITY, HSINCHU, TAIWAN (SUMMER 2016)

- Modeled and profiled a novel network on chip routing scheme in GEM5
- Engaged in research and collaboration in an international setting

INTEL CORPORATION, FOLSOM, CA (SUMMER - FALL 2014)

- Evaluated several code coverage tools and advised a purchase on the order of $10,000 based on this evaluation
- Built automated code coverage analysis infrastructure from scratch
- Proposed and implemented methods to accelerate testing through parallelization and pipelining

ARGONNE NATIONAL LABORATORY, DARIEN, IL (SUMMER 2013)

- Contributed to the software used by physicists for the analysis of data collected by the ATLAS detector at the Large Hadron Collider
- Utilized tools like source browsing and version control to work with a 12 year old code base with over one million lines of C++

RESEARCH

PROFESSOR DEMING CHEN'S GROUP (SPRING 2014 - CURRENT)
INDEPENDENT STUDY AND SENIOR THESIS

- Attended weekly research meetings, attended biweekly meetings with collaborators at Intel and Colorado State University, read papers, aided in peer reviewing a conference paper
- Currently working on running machine learning kernels on FPGAs using high level synthesis

SKILLS

C/C++

- Utilized tools such as GDB, Intel VTune Amplifier, Eclipse IDE, and IntelliJ IDE
- Experience with cache, vector, parallel (pthread and OpenMP) optimizations

Languages

- Proficient with Python, experienced with MATLAB
- Various functional, web, scripting, markup, and assembly languages

Tools

- Digital IC layout with Cadence Virtuoso, SPICE modeling
- RTL development and simulation for FPGA with Quartus
- GEM5 architecture modeling
- LLVM compiler infrastructure

COURSES

Logic Synthesis, Programming Languages, VLSI, Digital IC Design, Algorithms, Computer Architecture, Graph Theory, Compiler Construction, Numerical Analysis, Digital Signal Processing